

ABSTRACT OF THE DISCLOSURE

A signal processing apparatus using a plurality of microcomputers and a shared ROM. A microcomputer-A is connected to a microcomputer-B by way of a serial interface and a GPIO signal line. A flash ROM incorporated in the microcomputer-A has a program memory map corresponding to the microcomputer-A, wherein a run start address of the microcomputer-B, a program data size and program data therefor are disposed in a parameter table area of the program memory map corresponding to the microcomputer-A. Upon power-up, the microcomputer-A transfers data to the microcomputer-B via the serial interface, whereupon the microcomputer-B executes signal processing in the ordinary operation mode.